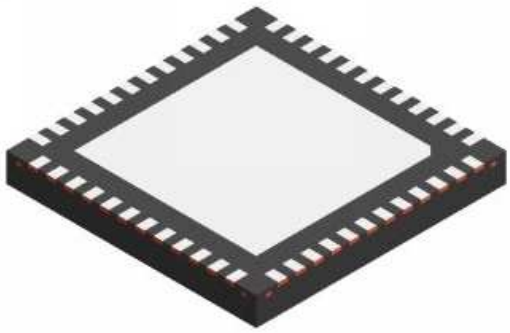
3-Phase Micro-motor Driver

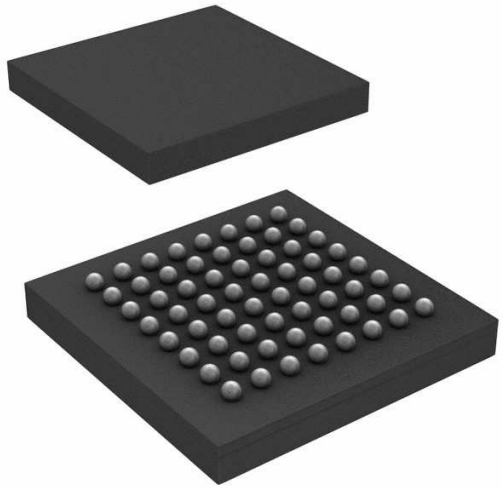
Features

- Three channel half bridge motor drivers
- Voltage booster to provide gate voltage for high side driving transistors
- 3x Low input offset, high common mode input voltage range, programmable gain sense amplifiers
- On chip 3.3V linear regulator
- 5V regulator for on-chip analog circuits
- Analog temperature sensor output
- Analog comparator
- Fault condition indicator
- Output over-current protection
- Thermal Protection

QFN 48 6x6



8x8 solder bump CSP



1 Introduction

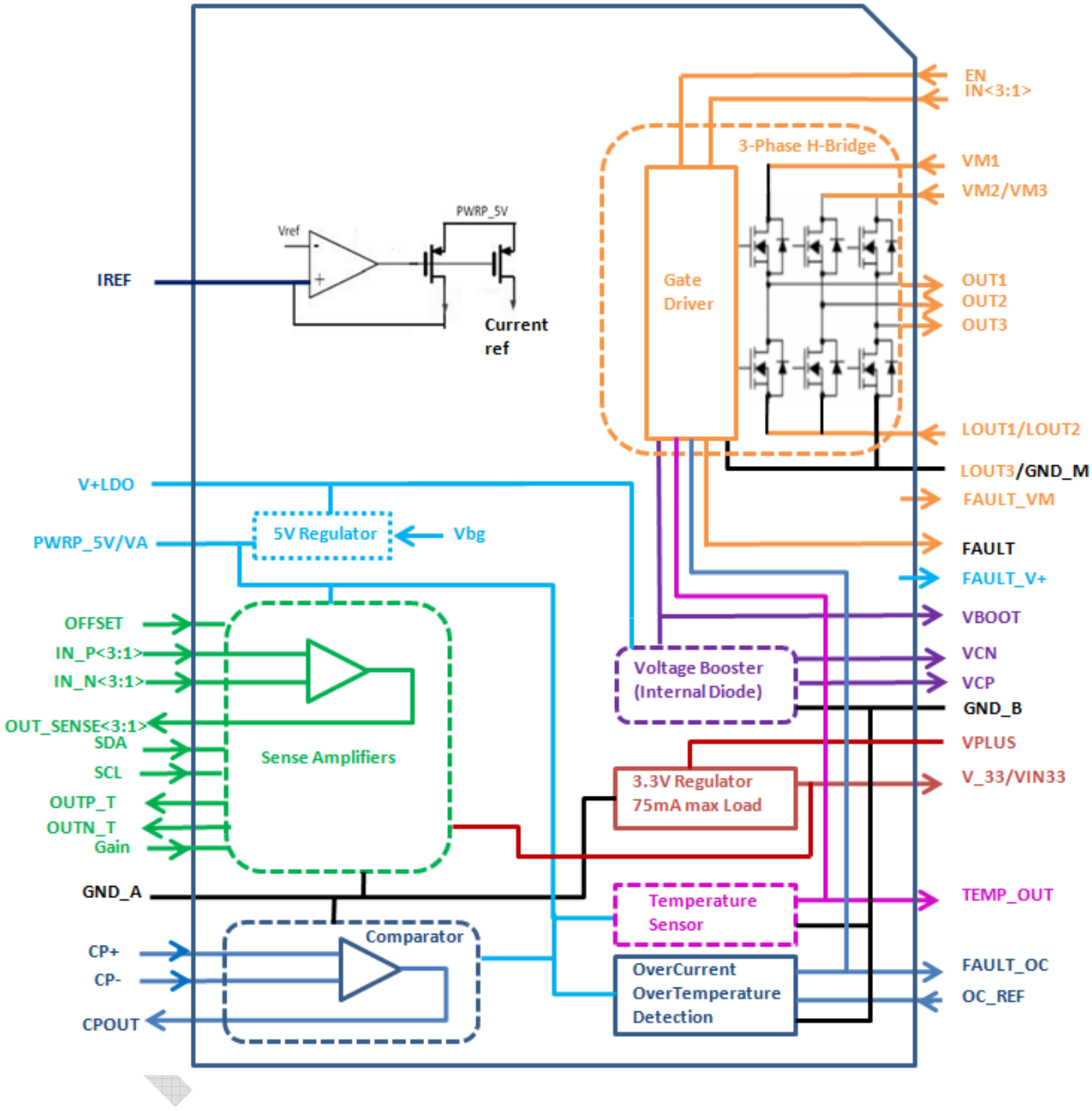
This device is an integrated 3-phase motor driver ASIC provides three individually controllable half-H-bridge drivers. It has built-in voltage regulators, gain controllable differential sense amplifiers and analog comparator. Each output driver channel consists of power MOSFETs in a half-H-bridge configuration.

It can supply up to 3A peak output current per half-H-bridge and provides internal shutdown functions for over-temperature and over-current protection.

Packaging

- Suggested package: 48 LEAD QUAD FLAT NO-LEAD PACKAGE, QFN 6x6x0.8, pitch 0.4mm.
- 8 x 8 solder bump CSP

Functional block diagram



2 Functional description

Output Stage

The device contains three half-H-bridge drivers. The source terminals of the low-side FETs of all three half-H bridges are tied together to DAP (Die Attach Pad) of QFN48 package.

Bridge Control

For each channel x, the corresponding INx input pin directly control the state (high or low) of the OUTx output. All three channels will be disabled by one enable pin EN. Table 1 shows the logic:

INx	EN	OUTx
X	0	Z
0	1	L
1	1	H

Table 1. Output state

Sense Amplifier

The Sense Amplifier amplifies and filters small differential signals in the presence of high common mode voltages for unidirectional and bidirectional current sensing. It has two selectable gains 50x or 75x, by one control input (GAIN)

GAIN	Sense amplifier gain
0	50
1	75

Table 2. Gain table of sense amplifiers

Analog Comparator

The device includes an analog comparator, which can find use as a current-limit comparator or for other purposes.

Power Management

The device has integrated two on-chip voltage regulators (3.3V and 5V) and a voltage booster for high voltage H-bridge gate voltage.

Biasing Circuits

- **IREF, Internal current reference**

To maintain a relatively temperature independent current reference for on-chip over-current protection circuit and other building blocks, an external resistor connecting between IREF (pin37 on QFN48 package or ball A1 on CSP) and ground will generate a reference current by:

$IREF = V_{IREF} / R_{IREF}$

Since the voltage at pin IREF is clamped to 1V by internal circuit, using an 100kohm resistor will give a reference current of 10μA. This will set the internal Over-Current limit to 3A.

- **OC_REF, External Over-Current Protection setting**

To provide a flexibility for the Over-Current sensing threshold, an external resistor connected between pin OC_REF and ground can be used to provide a lower trip point (<3A) for the Over-Current Protection. Resistor value should be defined as follows:

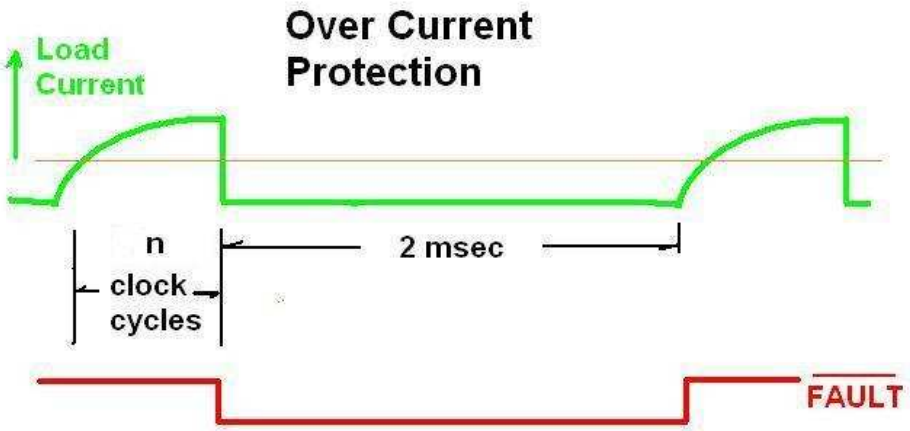
R_{OC_REF} = 18Kohm / I_{OC}, where I_{OC} is the desired over-current limit less than 3A

Protection Circuits

The device has full protection against over-current and over-temperature events.

- **Over-current Protection (OCP)**

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. The device disables the channel experiencing the over-current and drives the open drain FAULT\ pin low. When over-current condition on high-side devices (a short to ground, or across the motor winding) is detected for an accumulated clock pulse count of “n”, where n=$01 - $7F*note1, the chip will set off an over-current shutdown. Once OCP is triggered, the output drivers will stay in OFF state for 2msec while the FAULT\ signal will be generated accordingly. After the 2msec time-out, the FAULT pin will go tri-state and the drivers will be switched back ON. Should the Over-Current condition persist, the drivers will be turned off again. This will keep going until the MCU intervenes.



An up-down counter will be used to detect the over-current condition during the high side transistor is being turned on. Counter will advance by one when over-current condition is detected at the active edge of an internal clock cycle. It will go down by one if there is no over-current condition at the active clock edge. Over-current flag is set once the up-down counter arrives at a count of n. During count-down, the counter will stay at zero when all counts are removed. No underflow will be allowed on this counter.

Note1: The least significant bit of register $30 was negated during the design phase of the chip. So, for a desired count of "n"= b'1111111, the value of b'1111110 should be used. Default value of register $30 upon power up is b'0000000, which is equivalent to "n" = b'0000001. Setting register $30 to b'0000001 (i.e. "n" = 0) will turn off the OCP circuit.

- **Thermal Shutdown (TSD)**

If the die temperature exceeds safe limits (~165°C), the device disables all outputs and drives the FAULT\ pin LOW. Once the die temperature has fallen to a safe level (~155°C), operation automatically resumes.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDD	DC supply voltage	13	V
T_{op}	Operating temperature	0 to 70	°C
T_j	Junction temperature	–40 to 160	°C
T_{stg}	Storage temperature	–40 to 160	°C
HBM	ESD Susceptibility	2000	V
CDM	ESD Susceptibility	500	V

3.2 Thermal data

Table 4. Thermal data (QFN48 6x6)

Symbol	Parameter	Min	Typ	Max	Unit
θja	Junction to ambient thermal resistance, still air; soldered to PCB of FR-4 material. Heat sinking pad size on the 4 layer PCB is 3.8mm x 3.8mm with 7 thermal vias		35		°C/W
			TBD		

3.3 Electrical Characteristics

Unless otherwise stated, the results in *Table 5* below are given for the conditions: V+_LDO = 8 V, and T_A = 25 °C.

Symbol	Parameter	Testing condition	Min	Typ	Max	Unit
H-Bridge						
VMotor	H-Bridge supply voltage		5.5		12	V
	Logic inputs voltage range				3.3	V
Iout	RMS output current				1.75	A
Fsw	Switching frequency				100	kHz
RDS(on)	High-side / low-side switch ON resistance	TJ =125 °C			0.5	Ω
IDSS	Leakage current (Both transistors are off)				10	µA

	Output rise time		40		250	ns
	Output fall time		40		250	ns
t_{DT}	Dead time				0.5	µs
	Over-current protection threshold (peak)			3		A
Sense Amplifier						
Gain	Overall gain	Refer to table 2 for Gain setting	50		75	V/V
PSRR	Power Supply Ripple Rejection Ratio		65			dB
	Input offset voltage				1	mV
BW	Bandwidth	Gain=50	36			kHz
Rcm	Input Impedance Common Mode	−2V ≤ VCM ≤ 15V	120		350	kΩ
Rdm	Input Impedance Differential Mode	−2V ≤ VCM ≤ 15V	240		700	kΩ
DC CMRR	DC Common Mode Rejection Ratio		70		96	dB
AC CMRR	AC Common Mode Rejection Ratio	f = 1 kHz, at Gain=50		65		dB
CMVR	Input Common Mode Voltage Range		−2		15	V
OUT_Sense	Output voltage swing	RL = 100 kΩ	0.2		Vin33-0.2	V
VOFFSET	OFFSET pin voltage		2.5		3.5	V
Rout	Output resistance				5K	Ω
3.3V Regulator						
V+	Input voltage		4.5		16	V
	Output voltage		3.2		3.4	V
	Ripple rejection	Vripple = 1 Vrms, fripple = 120 Hz	−40			dB
I_{LOAD}	Output current				75	mA

LDO regulator						
V+_LDO			6		12	V
VLDO5V	Output voltage			5		V
ILDO5V	Load current				10	mA
Voltage Booster						
Vboot	Bootstrap voltage needed for driving the upper Power MOSFETs			VMotor + VLDO5V		V
Analog comparator						
VCPCM	Common mode voltage at the comparator inputs		0		3.3	V
	Propagation delay	Input over drive=50mV			500	ns
Thermal Protection						
	Thermal shutdown	Across all process corners	150	160	170	°C
	Thermal shutdown hysteresis			10		°C
Temperature sensor output						
V_{TEMP_OUT}		150°C		0.35		V
V_{TEMP_OUT}		0°C		0.7		V
Cload					10	pF
Iout, High	Output source current	VLDO5V=5V	250			µA
Iout, Low	Output sink current	At room temperature	130			µA
Rout	Output resistance				5K	Ω
ESD Immunity						
VESD	Electrostatic Discharge	HBM	-2		2	kV
		CDM	-500		500	V
	Latch-up JESD78D					

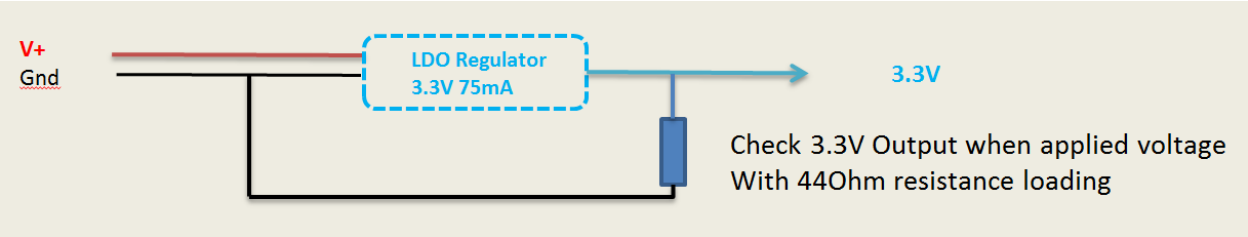
Miscellaneous input / output pins						
V_{OL}	Open drain output • FAULT, over-current and over temperature flag • CPOUT, analog comparator output • FAULT_OC, 2nd over-current flag	10K pull up to 3.3V			0.3	V
Ioff	Leakage current, Open drain output • FAULT, over-current and over temperature flag • CPOUT, analog comparator output • FAULT_OC, 2nd over-current flag	Output off state, tied to 3.3V			5	µA
UVLO						
$V_{UVLO\_V+\_LDO}$	Under Voltage Lock Out	V+_LDO		4.8		V
	hysteresis			0.4		V
V_{UVLO_VM}	Under Voltage Lock Out	Vmotor		4.9		V
	hysteresis			0.4		V
Power Dissipation						
	Power Dissipation per channel	H-Bridge FET rds on = 0.2Ω, Iout=1.75A;		1.85		W

Table 5. Electrical specifications

6 Testing

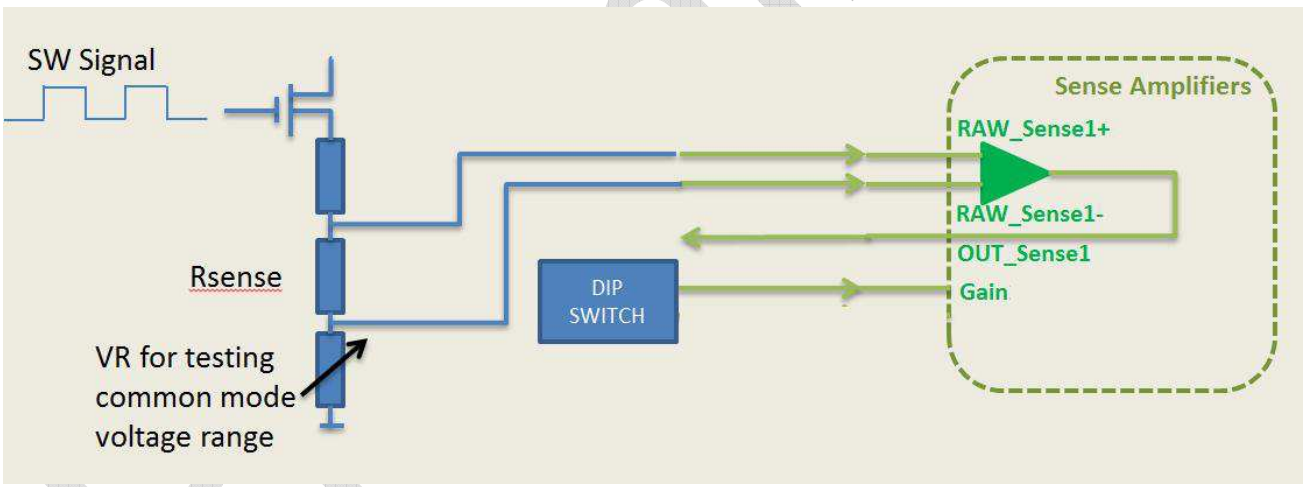
Each functional block can be fully tested individually.

- **3.3V Linear Regulator**

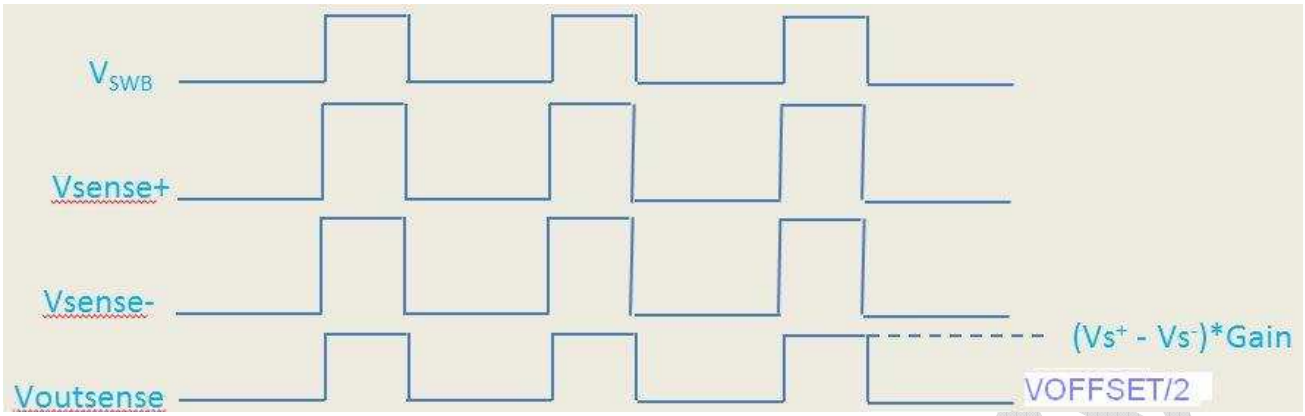


On chip 3.3V linear regulator to provide load current at 75mA maximum. Maximum input voltage to the regulator is 16V. However, application circuit must take care of the excessive power dissipation when high supply voltage and high loading current turn up at the same time.

- **Sense amplifier**

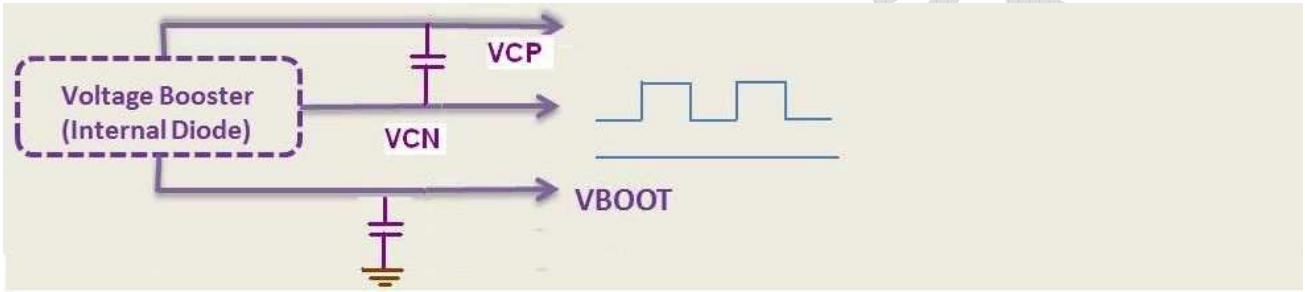


To avoid signal clipping at the output, input signals applied between “Raw_Sense+” and “Raw_Sense-“ have to be amplitude limited to (VOFFSET/2)÷Gain. Where Gain is selected according to input states defined in table 2.

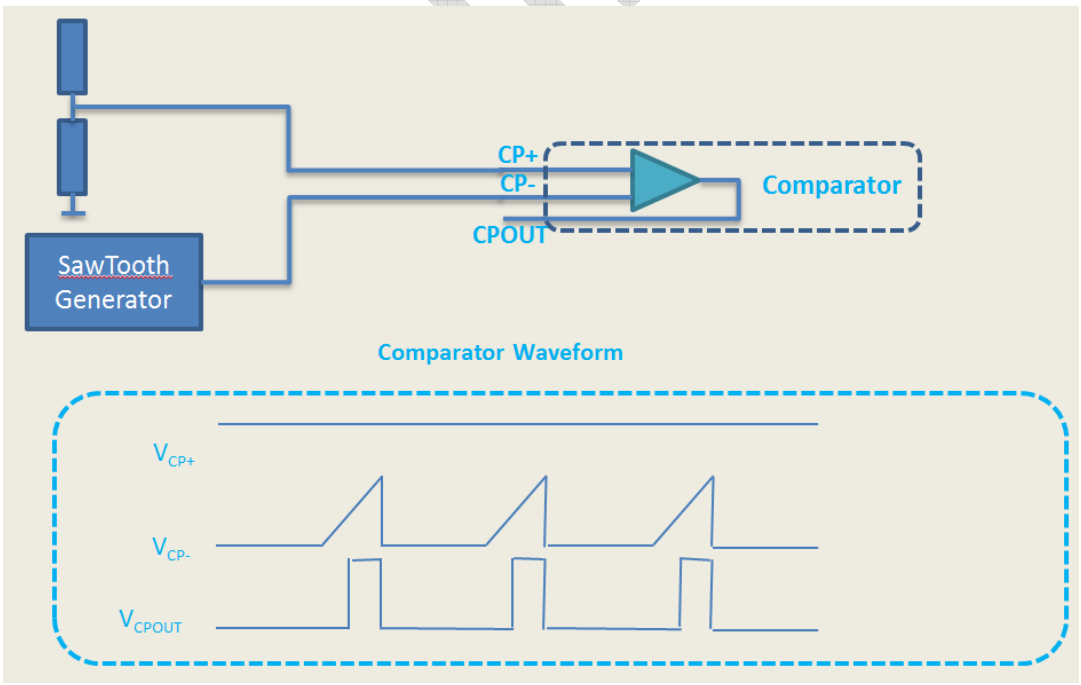


Sense Amplifier operating waveform

-Voltage Booster

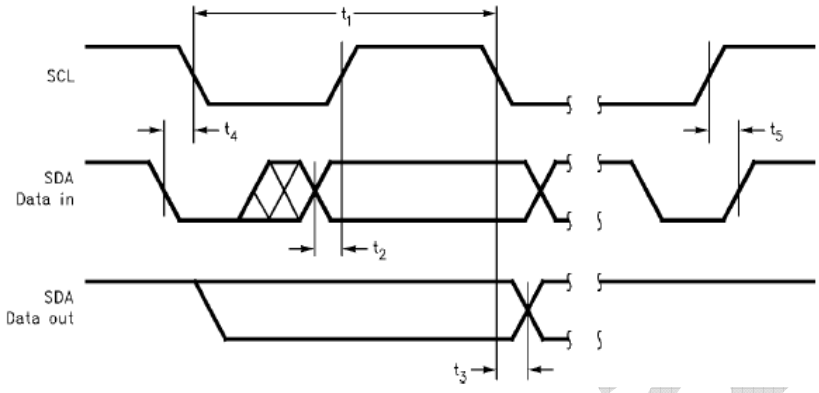


-Analog comparator



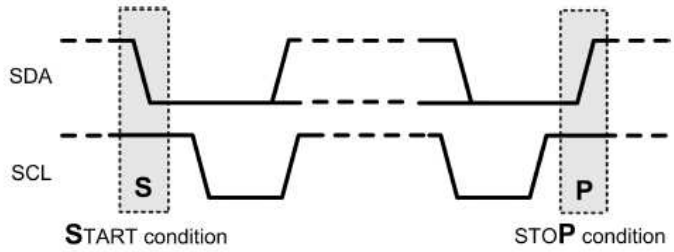
7 Serial Interface and Register table

Trimming of sense amplifiers are controlled through a serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). They are pulled-up to the logic 'high' level by resistors connect to a +3.3V. AP9961 support the write operation only at a clock rate up to 400kHz.



Serial interface timing diagram

Data on the SDA line must be stable during HIGH period of SCL. Each transmission sequence is framed by a START condition and a STOP condition.



START and STOP condition of serial interface

Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

AP9961 device address is 0111100

The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on bus that a device address is being written to the bus.

The 7-bit device address, 0111100, is written to the bus, the most significant bit (MSB) first, followed by the R/W bit. R/W bit=0 indicates the master is writing to the slave device.

	B7	B6	B5	B4	B3	B2	B1	B0 (R/W)
Device address	0	1	1	1	1	0	0	0

The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock

pulse is generated by the slave device. If AP9961 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, AP9961 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high.

The Serial Interface Software Protocol

1. START condition
2. Chip address ($78)
3. Register 1 address
4. Register 1 data
5. Register 2 address [Optionally, send any further data bytes]
6. Register 2 data [Optionally, send any further data bytes]

   .....
7. STOP condition