10W+10W FILTER-LESS STEREO CLASS-D AUDIO POWER AMPLIFIER

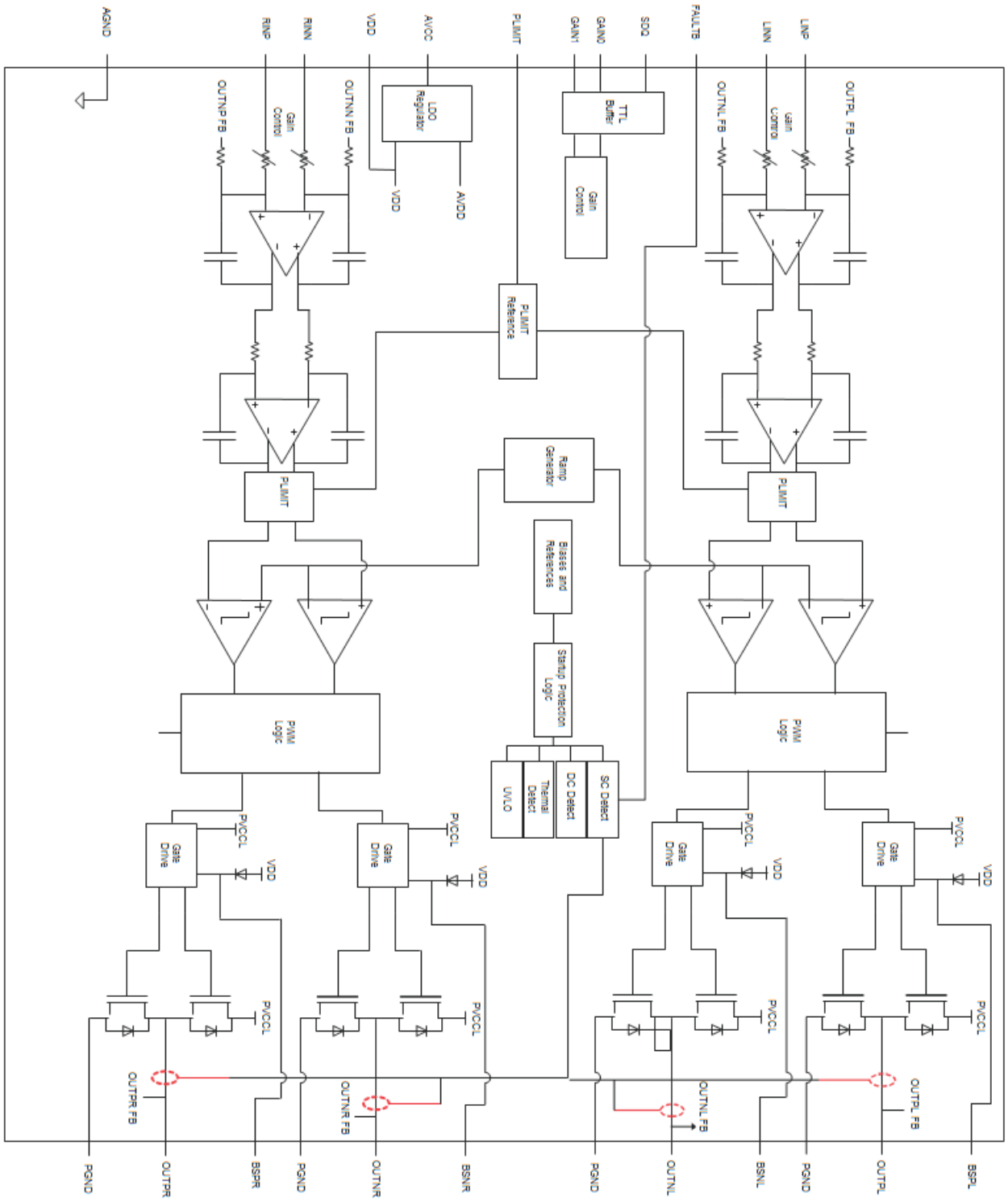
Features

- 10W/ch into an 8-Ω Load at 10% THD+N from a 12V Supply
- 87% Efficient Class-D Operation eliminates need for Heat Sinks
- Wide Supply Voltage Range Allows Operation from 8 V to 15 V
- Filter-Free Operation
- Speaker Protection Includes Adjustable Power Limiter plus DC Protection
- Short Circuit Protection and Thermal Protection with Auto Recovery Option
- Excellent THD+N / Pop-Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

Description

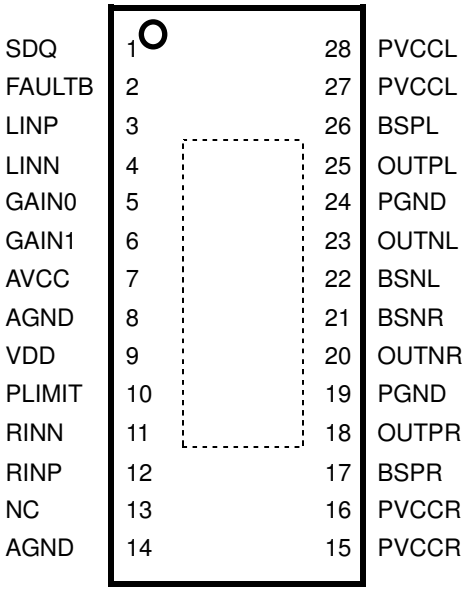
AM3823A is a Class-D audio power amplifier for driving stereo speakers in bridged-tied load (BTL) configuration. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. Speaker protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs. The AM3823A can drive stereo speakers as low as 4Ω. The high efficiency of the AM3823A, 87%, eliminates the need for an external heat sink when playing music. The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

1 Device block diagram



2 Pin description

2.1 Pin out



2.2 Pin out

PIN NAME	PIN NO	I/O/P	DESCRIPTION
SDQ	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
FAULTB			Open drain output to indicate short circuit or dc detect fault conditions. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to SDQ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel.
LINN	4	I	Negative audio input for left channel.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8		Analog signal ground
VDD	9	O	High-side FET gate drive supply. Nominal voltage is 5V. Also should be used as supply for PLIMIT function
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from VDD to GND to set power limit. Connect directly to VDD for no power limit.
RINN	11	I	Negative audio input for right channel.
RINP	12	I	Positive audio input for right channel.
NC	13		Not connected
AGND	14	I	Connect to AGND
PVCCR	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCR	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19		Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24		Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
PVCCL	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.

3 Electrical specifications

3.1 Absolute maximum ratings

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V to 15 V
V_I	Interface pin voltage	SDQ, GAIN0, GAIN1, FAULTB	–0.3 V to V_{CC} + 0.3 V
		PLIMIT, TM	–0.3 V to VDD + 0.3 V
		RINN, RINP, LINN, LINP	–0.3 V to 6.3 V
	Continuous total power dissipation		See Thermal Information
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
RL	Min Load Resistance	BTL	3.2
ESD	Electrostatic discharge	Human body model	±2 kV
		Charged-device model	±500 V

3.2 Thermal information

THERMAL METRIC		TSSOP28	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34	
θ_{JB}	Junction-to-board thermal resistance	18	

3.3 RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	15	V
V_{IH}	High-level input voltage	SDQ, GAIN0, GAIN1, NC	2		V
V_{IL}	Low-level input voltage	SDQ, GAIN0, GAIN1, NC		0.8	V
V_{OL}	Low-level output voltage	FAULTB, $R_{PULL-UP}$=100k, V_{CC}=15V		0.8	V
I_{IH}	High-level input current	SDQ, GAIN0, GAIN1, NC, V_I = 2V, V_{CC} = 12 V		50	µA
I_{IL}	Low-level input current	SDQ, GAIN0, GAIN1, NC, V_I = 0.8 V, V_{CC} = 12 V		5	µA
T_A	Operating free-air temperature		–40	85	°C

3.4 Electrical specifications

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETE		TEST CONDITIONS		MIN	TYP		UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	SDQ = 2 V, no load, PV_{CC} = 12V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown	SDQ = 0.8 V, no load, PV_{CC} = 12V			400		µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		380		mΩ
			Low side		260		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	SDQ = 2 V			14		ms
t_{OFF}	Turn-off time	SDQ = 0.8 V			200		µs
VDD	Gate Drive Supply	I_{VDD} = 2mA		4.5	5.0	5.5	V
V_O	Output Voltage maximum under PLIMIT	V(PLIMIT) = 2 V; V_I = 1V		4.5	5.2	5.9	V
t_{DCDET}	DC Detect time	V(RINN) = 6V, VRINP= 0V			420		ms

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 3 W (half-power)		0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		90		µV
	Crosstalk	P_O = 1 W, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		100		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal shut down trip point			150		°C
	Thermal hysteresis			15		°C

4 DEVICE INFORMATION

Gain Setting Via GAIN0 and GAIN1 Inputs

The gain of the AM3823A can be set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taping point between the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the AM3823A. At the lower gain settings, the input impedance could increase to as high as 60 kΩ

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

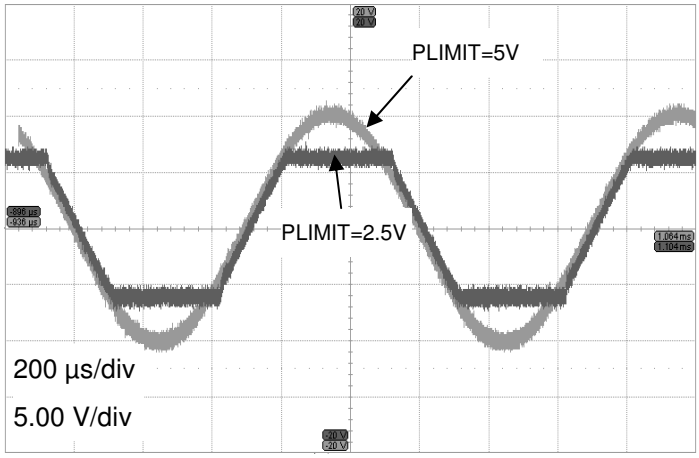
SDQ Operation

The AM3823A employs a shutdown mode of operation. It will reduce supply current (I_{CC}) to the absolute minimum level during idling periods for power conservation. The SDQ input terminal should be held high (see **DC Characteristics** for trip point) during normal operation when the amplifier is in use. Pulling SDQ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SDQ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

PLIMIT

The voltage at pin 10 can be used to limit the output power level. Add a resistor divider between VDD and ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also, an 1µF capacitor from pin 10 to ground is needed for decoupling.



PVCC=12V, Vin=1V,
RL=8Ω, Gain=20dB

The PLIMIT circuit sets a limit on the output peak-to-peak voltage (waveform shown was recorded after passing through output low pass filters). The power clipping is done by limiting the duty cycle to a fixed maximum value converted from the voltage level at pin PLIMIT. This limit can be thought of as a "virtual" voltage rail which is lower than the supply voltage at PVCC. This "virtual" rail is around 2 times the voltage at the PLIMIT pin.

Table 2. PLIMIT Typical Operation

PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB

PLIMIT VOLTAGE [V]	OUTPUT VOLTAGE VP-P [V]	OUTPUT POWER [W]
0.0	0.15	0.01
0.5	2.90	0.23
1.0	5.52	0.78
1.5	8.07	1.72
2.0	10.66	2.91
2.5	13.47	4.40
3.0	16.24	6.01
3.5	18.70	7.60
4.0	20.62	8.79
4.5	20.97	8.99
5.0	21.05	9.03

PVCC=12V, Vin=1Vrms, RL=4Ω, Gain=20dB

PLIMIT VOLTAGE [V]	OUTPUT VOLTAGE VP-P [V]	OUTPUT POWER [W]
0.0	0.13	0.00
0.5	2.40	0.31
1.0	4.80	1.22
1.5	7.31	2.71
2.0	9.90	4.77
2.5	12.69	7.36
3.0	15.19	10.15
3.5	17.16	12.42
4.0	18.84	14.37
4.5	19.05	14.61
5.0	19.11	14.67

VDD

The VDD Supply is generated on the chip to provide the gate drive for the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1µF capacitor to ground at this pin for decoupling.

DC DETECT

AM3823A has circuitry to protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will trigger the FAULTB pin to go low. The DC Detect fault will also cause the amplifier to enter shutdown mode under which the outputs will go Hi-Z. To clear the DC Detect fault, it is necessary to cycle the PVCC supply. Cycling SDQ will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, 57% -43%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid false trigger due to the DC detect circuit, hold the SDQ pin low at power-up until the signals at the inputs are stable. Also, special care must be taken to match the impedance seen from the positive and negative inputs.

The minimum differential input voltages required to trigger the DC detect are show in table 2. The inputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 3. DC Detect Threshold

AV(dB	Vin (mV, differential)
20	112
26	56
32	28
36	17

Short-Circuit Protection and Automatic Recovery Feature

AM3823A protects the output circuit from over current conditions due to short circuit. The short circuit protection fault is reported on the FAULTB pin as a low state. The amplifier outputs are switched to Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDQ pin through the low state.

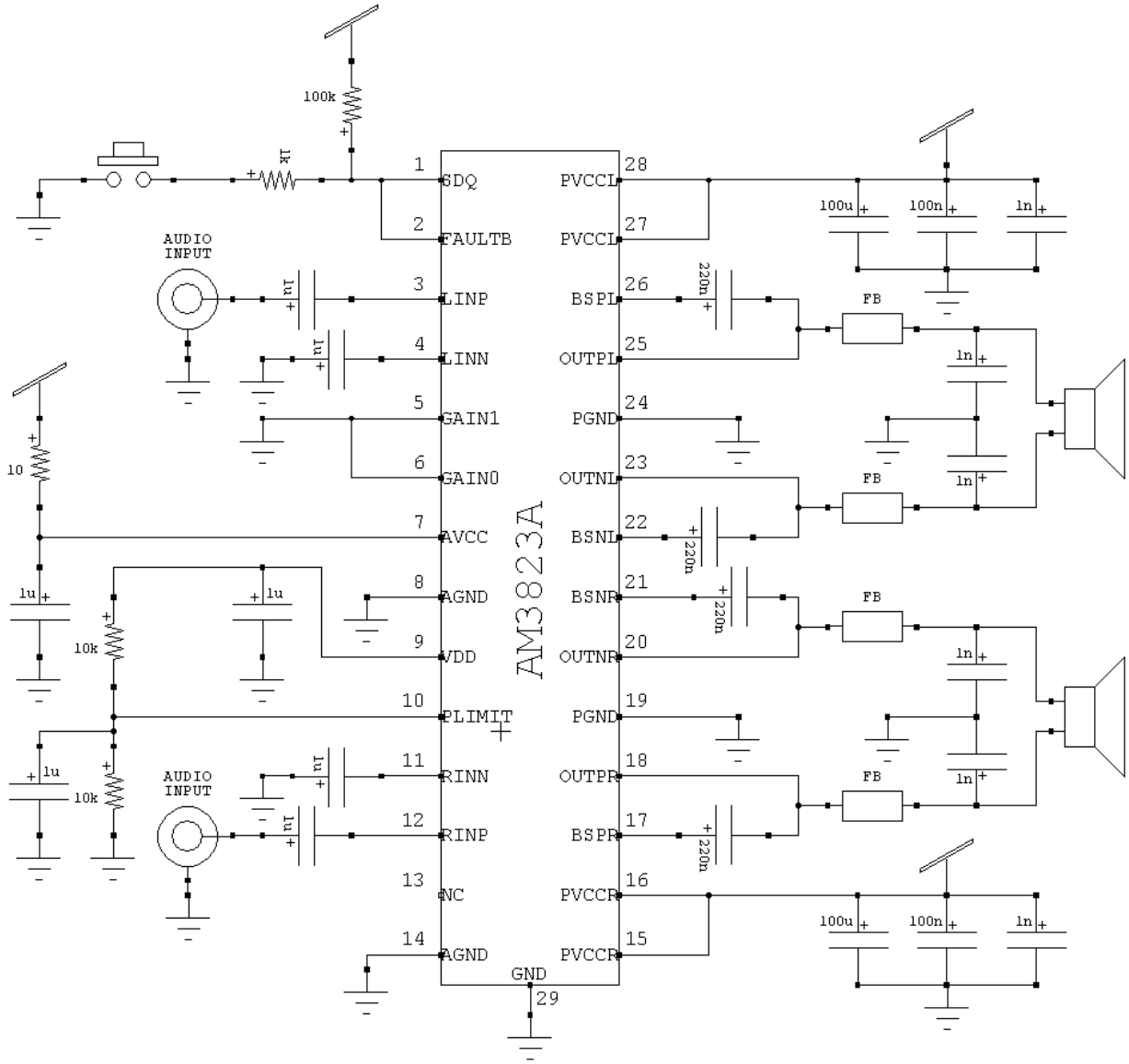
If automatic recovery from the short circuit protection latch is desired, connect the FAULTB pin directly to the SDQ pin. This allows the FAULTB pin function to automatically drive the SDQ pin low which clears the short-circuit protection latch.

Thermal Protection

Thermal protection on the AM3823A prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die drops by 15°C from the trip point. The device begins normal operation at this point with no external system interaction.

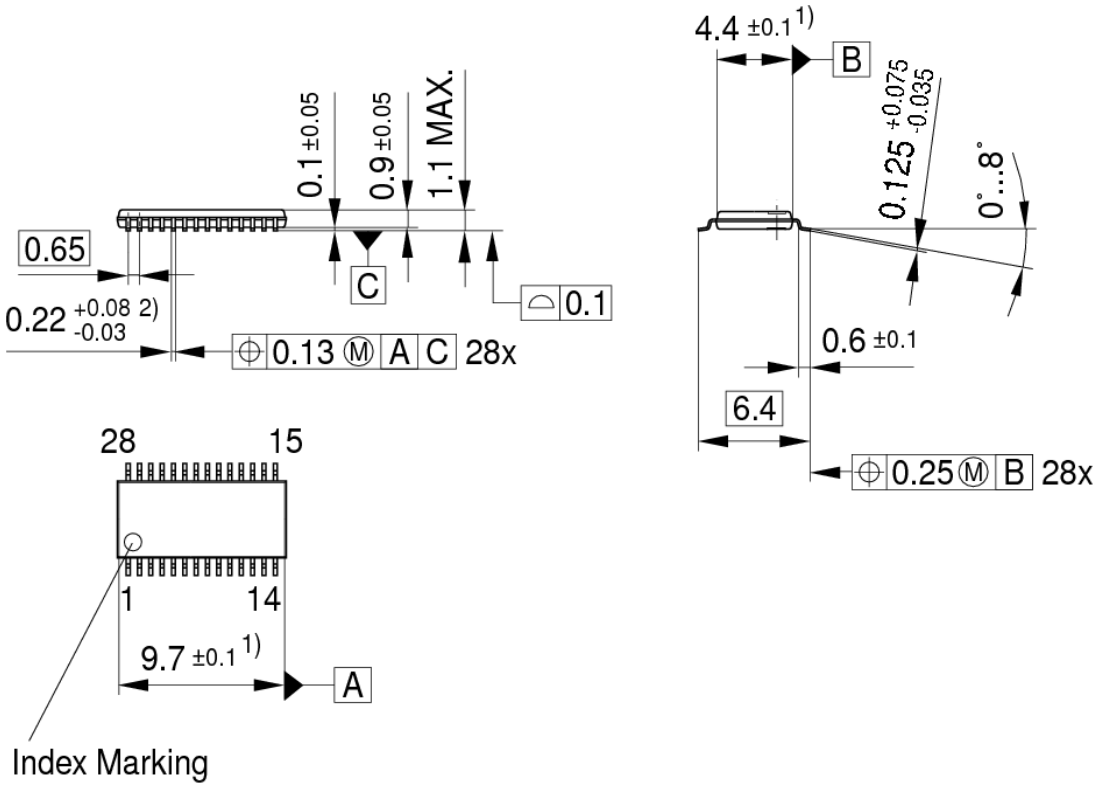
Thermal protection faults will have no effect on FAULTB pin.

5 Application circuit



6 Package Information

TSSOP28



Notes:

A. All linear dimensions are in millimeters.

B. Does not include plastic or metal protrusion of 0.15 max. per side

C. Does not include dambar protrusion of 0.08 max. per side